REMARKS/ARGUMENTS

The Applicants hereby respectfully request reconsideration of the present application in view of the foregoing amendments and the following remarks/arguments. Claims 1-20 were originally filed in the present application. By the prior Amendment, claims 1 and 11 were amended, and claims 21 and 22 were added. By the present Amendment, claims 1, 11 and 22 are amended. No claims have been canceled. Accordingly, claims 1-22, as herein amended, are now pending in the present application.

I.   OBJECTIONS

The Examiner has objected to claim 22 for containing a typographical error. In response, the Applicants have amended claim 22 to correct this inadvertent error.

II.   REJECTIONS UNDER 37 C.F.R. §102

The Office Action has rejected claims 1, 4, 6-7, 9-11, 14, 16-17 and 19-22 under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 5,646,545 to Trimberger *et al.* In addition to the amendments and arguments provided in the prior Amendment, the Applicants have further amended independent claims 1 and 11 in the present Amendment. Specifically, claims 1 and 11 have been amended to recite: (1) that the plurality of data storage units "are located outside the logic computing units," and (2) that "another of said plurality of configuration data modules is being retrieved from outside the logic computing *system*."

In contrast to present claims 1 and 11, Trimburger, for example in his Abstract, clearly teaches that the PLD comprises a plurality of configurable logic blocks (CLBs). Therefore, it is clear by Trimburgers explicit statements that the programmed CLBs are located *inside the PLD*. In addition, Trimburger, at col. 6, lns. 24-50, discloses an FPGA that replaces the conventional transistor memory cell (five transistor (5T) memory cell 100), which provides control for all logic functions on the FPGA chip, with a bit set having

multiple memory cells (8 in the preferred embodiment). On the other hand, Trimburger does not teach or suggest a plurality of data storage units located outside a logic computing unit. Accordingly, Trimburger requires the construction of an entirely new, and likely costly, FPGA's logic circuit. In contrast, the present claims provide a logic system (and related method) having the plurality of data storage units (41a to 41d, 49a to 49d) located outside the logic computing unit (43). In this structure, a conventional logic circuit (such as a conventional FPGA's logic circuit having only single memory cells) can be used as the logic computing unit (43). Thus, the need and cost for creating newly logic circuit is decreased or more likely eliminated.

For at least these reasons, the Applicants respectfully believe that the Examiner has not fully understood the teachings of Trimburger, as well as the context of those teachings. Trimberger teaches: (1) constructing multiple configuration memory cells in place of the conventionally used single memory cell, and then (2) configuring select ones of these memory cells that are not currently being used for computing in advance of their use in future logic computations. Accordingly, Trimberger is directed to increasing logic density by using multiple memory cells in place of single memory cells, typically at the expense of processing speed. (See, e.g., col. 22, lns. 62-64, and col. 23, lns. 65-67). In contrast, the present claims provide faster processing using the "behind-the-scenes" (i.e., while the logic circuits of the FPGA are computing) retrieving and storing of future-needed configuration data from off-chip data stores into on-chip data modules that are quickly and directly accessible by the FPGA hardware when reconfiguration of the conventional logic circuit is needed for continued program execution. Thus, the need for greater logic density is decreased because of the increased processing speed capable from the conventional logic circuits in the logic computing unit. The Examiner has responded to the Applicants' placing of Trimburger's teaching in context by dismissing these remarks as "immaterial" and "not represented in the

claim language." However, the context is material to an understanding of the circuit structure taught by Trimburger, and whether they can or cannot provide certain features. Stated another way, if a certain circuit structure is needed to provide certain features, and those circuit structures could not provide other features, the context of the teachings of a reference is material to help explain that reference's circuit structure.

For at least the above reasons, Trimburger does not disclose all of the elements of independent claims 1 and 11, as herein amended, nor the claims dependent thereon. Thus, Trimberger does not anticipate independent claims 1 and 11, of their dependent claims. Accordingly, the Applicants respectfully request that this rejection be withdrawn.

III.   REJECTIONS UNDER 35 U.S.C §103

The Office Action has rejected dependent claims 2 and 12 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of U.S. Patent 5,036,473 to Butts *et al.* In addition, the Office Action has rejected dependent claims 3 and 13 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of Butts, and further in view of article drafted by Liu *et al.* Next, the Office Action has rejected dependent claims 5 and 15 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of the Liu article. Also, the Office Action has rejected dependent claims 8 and 18 under 35 U.S.C §103(a) as allegedly obvious and thus unpatentable over Trimberger in view of the article drafted by Patterson *et al.*

The Applicants respectfully assert that all of these dependent claims are not obvious over the cited combinations of references.   As discussed above, Trimberger does not teach or suggest all of the elements recited in independent claims 1 and 11, as amended herein.   Moreover, the invention in claims 2 and 12 is characterized in that: (1)

a plurality of data storage units, which are located outside a logic computing unit, form a shift register; and (2) the logic computing unit refers to configuration data module(s) stored in one or more of the plurality of data storage units. Such structure enables, for example, determining a procedure of referring to the configuration data module(s) from the logic computing unit without any external planning. Thus, the process amount for configuring the logic computing unit is decreased.

In contrast, Butts, Liu, and Patterson do nothing to cure the deficiencies of Trimberger discussed above, and is only relied upon for teaching specific limitation set forth in these rejected dependent claims. Specifically, these secondary references are offered for the teaching of shift registers for holding configuration data (Butts), the circular shift of the data in the shift register (Liu), selecting configuration data from the shift register (Liu), and selecting from the shift register based on a call signal (Patterson). However, even assuming these elements are taught by these secondary references as set forth in the Office Action, the cited combinations still do not teach all of the limitations of claims 1 and 11, as discussed in detail above.

As a result, the combinations of Trimberger with Butts, Liu, and Patterson, or various combinations thereof, still do not teach or suggest all of the elements of independent claims 1 and 11. Since dependent claims 2 and 12, 3 and 13, 5 and 15, and 8-18 depend from independent claims 1 and 11, respectively, these dependent claims are also not obvious in view of the various cited combinations of references set forth in the rejections. Accordingly, the Applicants respectfully request that the Examiner also withdraw the §103(a) rejections with respect to the pending claims.

IV.   CONCLUSION

The Applicants respectfully submit that the pending claims are in condition for allowance, and request a Notice of Allowability for the pending claims. The Examiner is invited to contact the undersigned Attorney of Record if such would expedite the prosecution of the present Application. The three-month response deadline expired on July 10, 2007. Thus, this Amendment is being submitted with the fee for a one-month Extension of Time to extend the response period to August 10, 2007. Accordingly, this Amendment is timely. In addition, this Amendment is being filed with a Request for Continued Examination, along with the required fee, so that the amendments and arguments submitted herein will be considered. If further fees are believed due, or an overpayment has occurred, the Director is authorized to charge or deposit any necessary fees to Deposit Account No. 13-0480, referencing the Attorney Docket specified herein.

Respectfully submitted,

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